AUTOMATIC GAIN CONTROL DEVICE

BACKGROUND OF THE INVENTION

Field of the invention

The invention relates to an automatic gain control (AGC) device, and more particularly to an AGC device without being influenced by leakage current.

Description of the Related Art

An automatic gain control (AGC) device generates an output signal with desired amplitude by providing a properly stable gain control voltage for input signals with different amplitudes. Referring to FIG. 1, a conventional AGC device 10 includes a variable gain amplifier (VGA) 11, a top detector 12, a bottom detector 13, a substractor 14, a target setting unit 15, a comparator 16, a charge pump 17, and a capacitor 18. The control device 10 outputs an output signal Vo from the VGA 11, which gain is controlled by the gain control voltage Vg. The top detector 12 and the bottom detector 13 detect a top voltage Vt and a bottom voltage Vb of the output signal Vo. The substractor 14 calculates a voltage difference Vd between the top voltage Vt and the bottom voltage Vb, wherein the voltage difference Vd is a peak-to-peak amplitude of the output signal Vo. Thereafter, the comparator 16 compares the voltage difference Vd with a target value Vs and then generates a comparison value which control the charge pump 17 to generate a gain control voltage Vg and holds the voltage by the capacitor 18. The operation principle is described in the following. When the comparison value is HIGH, the voltage difference Vd is smaller than the target value Vs. At this time, the charge pump 17

charges the capacitor 18 to increase the gain control voltage Vg. In this case, the gain of the VGA 11 increases, the voltage of the output signal Vo is increased, and the voltage difference Vd also is increased accordingly. The operation of the loop lasts until the voltage difference Vd equals to the target value Vs. On the contrary, if the voltage difference Vd is greater than the target value Vs, the charge pump 17 discharges the capacitor 18 to reduce the gain control voltage Vg. Therefore, the gain of the VGA 11 is dropped to decrease the voltage of the output signal Vo, and the voltage difference Vd is also decreased. The operation of the loop lasts until the voltage difference Vd equals to the target value Vs.

The control device 10 utilizes the charge pump 17 to constitute a closed loop and build a optimum gain control voltage on the capacitor 18 to set an optimum gain control. In some occasions (e.g., in a long-time seeking of an optical storage system), the input signal's amplitude to the VGA 11 is un-regular, then, the loop has to be disabled and the gain control voltage Vg then has to be held for a period of time in order to avoid error operations of the AGC device. In this case, the AGC voltage may be dropped due to the leakage current of the capacitor 18, and the held gain may be changed to cause errors in system operations.

SUMMARY OF THE INVENTION

In view of the above-mentioned problems, an object of the invention is to provide an AGC device, which is free from being influenced by leakage current and capable of holding the gain control voltage for a long time.

To achieve the above-mentioned object, the invention provides an AGC device including a first control loop, a second control loop, and a multiplexer. The first

control loop receives an input signal and generates a first AGC voltage accordingly. The second control loop receives the first AGC voltage, registers the first AGC voltage in a digital format, and outputs a second AGC voltage. The multiplexer chooses the first AGC voltage or the second AGC voltage as an AGC voltage according to a holding signal.

The second control loop includes a second comparator, an up/down counter, a digital-to-analog converter (DAC), a hold control unit, and a counting signal generator. The second comparator has a positive terminal for receiving the first AGC voltage and a negative terminal for receiving the second AGC voltage, and outputs a comparison signal. The up/down counter receives a comparison signal as an up/down counting control signal, up-counts when the comparator outputs HIGH, down-counts when the comparator outputs LOW, receives a counting signal as a counting trigger signal for counting, and outputs a count value accordingly. The DAC converts digital data of the count value into the second AGC voltage. The hold control unit generates the hold signal according to a hold command. The counting signal generator receives the hold signal, stops generating the counting signal to hold the result of the counter when the hold signal is LOW and enabled, and restores the counting signal to make the counter count normally when the hold signal is disabled.

Since the second control loop registers the first AGC voltage value in a digital format, only the second AGC voltage has to be output when the AGC voltage has to be held.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a conventional AGC device.

FIG. 2 shows a block diagram of a first loop of the AGC device of the present invention.

FIG. 3 shows a block diagram of a second loop of the AGC device of the present invention.

FIG. 4 is a schematic illustration showing a relationship between the DAC output voltage and the gain control voltage of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The AGC device of the invention will be described with reference to the accompanying drawings.

Since the gain control voltage is held by a capacitor in a typical AGC device, the held gain control voltage may drop owing to the leakage current of the capacitor in the application of holding for a long time. Consequently, the invention proposes an AGC device utilizing a second loop circuit to register digitized voltage values so as to hold the gain control voltage and keep it unchanged for a long time.

FIGS. 2 and 3 show block diagrams of the AGC device of the invention, wherein FIG. 2 shows a first control loop while FIG. 3 shows a second control loop. The first control loop 20 includes a variable gain amplifier (VGA) 11, a top detector 12, a bottom detector 13, a substractor 14, a target setting unit 15, a comparator 16, a charge pump 17, a capacitor 18, a programmable low pass filter (PLPF) 22, and a multiplexer 21. The first control loop 20 is substantially the same as that of the conventional AGC device 10 except for the difference residing in that the multiplexer 21 is used to choose a gain control voltage of the first loop or the second

loop as the gain control voltage. Since the units such as the variable gain amplifier 11, a top detector 12, a bottom detector 13, a substractor 14, a target setting unit 15, a comparator 16, a charge pump 17, a capacitor 18, and the like of the first control loop 20 have the same functions as the prior art, detailed descriptions thereof will be omitted. The first control loop 20 utilizes the PLPF 22 to filter a first gain control voltage held by the capacitor 18.

Referring to FIG. 3, the second control loop 30 includes a comparator 31, an up/down counter 32, a protect logic 33, a digital-to-analog converter (DAC) 34, an AND gate 35, a hold control unit 36, and a clock frequency selector 37. The comparator 31 receives the output voltage from the PLPF 22 and the output voltage from the DAC 34, outputs HIGH when the output voltage of the PLPF 22 is higher than that of the DAC 34, and outputs LOW when the output voltage of the PLPF 22 is lower than that of the DAC 34. The counter 32 is an up/down counter for receiving the output signal of the comparator 31 and the counting signal of the AND gate 35. When the comparator 31 outputs HIGH, the counter 32 up-counts the pulse number of the counting signal; when the comparator 31 outputs LOW, the counter 32 down-counts the pulse number of the counting signal. When the hold signal is enabled, there is not any pulse in the counting signal and the count value of the counter 32 is held unchanged. The protect logic 33 receives the count value of the counter 32 and protects the count value from overflowing. For example, if the counter 32 is a 6-bit counter, when the count value is 111111 and the counter 32 still up-counts, the count value changes to 000000. Thus, the protect logic 33 will protect the count value. Of course, if the output range of the DAC is greater than the variation range of the gain control voltage Vc of the VGA 11 under different gain

requirements, the protect logic 33 can be omitted. The DAC 34 receives the output value authenticated by the protect logic 33, converts it into the analog second AGC voltage, and then outputs the second AGC voltage to the comparator 31 and the multiplexer 21.

The hold control unit 36 receives a hold command of the system and controls the hold signal according to the hold command. That is, when the hold command is to hold the gain control voltage, the hold control unit 36 outputs LOW to enable the hold signal; and when the hold command is to immediately respond the gain control voltage, the hold control unit 36 outputs HIGH to disable the hold signal. The clock frequency selector 37 receives a reference clock and divides the frequency of the reference clock into the counting clock with desired frequency. The AND gate 35 receives the counting clock of the hold signal, outputs the counting clock when the hold signal is disabled, and outputs LOW to hold the result of the counter when the hold signal is enabled. Thus, when the hold signal is disabled, the counter 32 counts up or down according to the counting signal to make the output voltage of the DAC 34 almost equal to the output voltage (first gain control voltage) of the PLPF 22. On the other hand, when the hold signal is enabled, the value of the counter 32 is kept unchanged. Thus, the output voltage of the DAC 34 is also held constant so that the AGC voltage is held unchanged.

When the hold signal is disabled, the multiplexer 21 outputs the first gain control voltage of the PLPF 22 to the VGA 11. Thus, the operation of the first control loop is the same as that of the conventional AGC device (FIG. 1) in this stage. When the hold signal is enabled, the multiplexer 21 outputs the second gain control voltage of the DAC 34 of second control loop 30 to the VGA 11. In this state, since

the input value of the DAC 34 is held unchanged, the voltage output to the VGA 11 is held constant without dropping owing to the leakage current of the capacitor 18.

FIG. 4 is a schematic illustration showing a relationship between the output voltage of the DAC 34 and the AGC voltage of the invention. As shown in the drawing, when the AGC device starts operating, the output voltage of the DAC 34 will follow the variation of the AGC voltage because the hold signal is disabled. At the beginning, the loop of the AGC is not stable yet. Then, the gain control voltage Vc of the AGC changes gradually until it converges at a stable voltage value. Under the control of the up/down counter of the second loop 30, the output voltage of the DAC 34 follows the variation of the voltage (gain control voltage) Vc output from the PLPF 22, and finally approaches to voltage Vc output from the PLPF 22. When the hold command is to hold the AGC voltage, the hold control unit 36 enables the hold signal and the counter 32 stops counting. Thus, the voltage of the DAC 34 is held constant. Meanwhile, the multiplexer 21 outputs the second gain control voltage of the DAC 34 to the VGA 11 in order to make the AGC voltage become the voltage of the DAC 34. Consequently, the AGC device of the invention can hold the AGC voltage for a long time.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific construction and arrangement shown and described, since various other modifications may occur to those ordinarily skilled in the art.